CLAIMS

What is claimed is:

1. A method for dynamically programming Field Programmable Gate Arrays (FPGA) in a coprocessor, the coprocessor coupled to a processor, the method comprising:

(a) beginning an execution of an application by the processor;

(b) receiving an instruction from the processor by the coprocessor to perform a function for the application;

(c) determining that the FPGA in the coprocessor is not programmed with logic for the function;

(d) fetching a configuration bit stream for the function; and

(e) programming the FPGA with the configuration bit stream.

2. The method of claim 1, wherein the issuing step (b) comprises:

(b1) receiving the instruction by an Auxiliary Processing Unit (APU) interface between the processor and the coprocessor.

3. The method of claim 2, wherein the determining step (c) comprises:

(c1) determining that the APU interface issued a faulty commit.

4. The method of claim 1, wherein the fetching step (d) comprises:

(d1) initiating an exception subroutine by the processor; and

(d2) fetching the configuration bit stream for the function by an exception

subroutine of the processor.

5. The method of claim 4, wherein the initiating step (d1) comprises:

(d1i) determining that the coprocessor issued a faulty commit; and

(d1ii) branching to the exception subroutine by the processor in response to the faulty commit.

6. The method of claim 4, wherein the fetching step (d2) comprises:

(d2i) decoding a function identifier by the exception subroutine;

(d2ii) requesting and being granted ownership of the function;

(d2iii) fetching the configuration bit stream for the function from a memory;

(d2iv) identifying an exception type and a coprocessor instruction type for the configuration bit stream; and

(d2v) sending the configuration bit stream to the coprocessor.

7. The method of claim 1, wherein the programming step (e) comprises:

(e1) performing a sequence of load and store instructions by an exception subroutine of the processor to program the FPGA with the configuration bit stream.

8. The method of claim 1, further comprising:

(f) receiving a reissuance of the instruction by the coprocessor.

9. A method for dynamically programming Field Programmable Gate Arrays (FPGA) in a coprocessor, the coprocessor coupled to a processor, the method comprising:

(a) beginning an execution of an application by the processor;

(b) receiving an instruction from the processor by the coprocessor to perform a function for the application;

(c) issuing a faulty commit when the FPGA in the coprocessor is not programmed with logic for the function;

(d) initiating an exception subroutine by the processor in response to the faulty commit;

(e) fetching a configuration bit stream for the function by the exception subroutine; and

(f) performing a sequence of load and store instructions by the exception subroutine to program the FPGA with the configuration bit stream.

10. A computer readable medium with program instruction for dynamically programming Field Programmable Gate Arrays (FPGA) in a coprocessor, the coprocessor coupled to a processor, comprising the instructions for:

(a) beginning an execution of an application by the processor;

(b) receiving an instruction from the processor by the coprocessor to perform a function for the application;

(c) determining that the FPGA in the coprocessor is not programmed with logic for the function;

(d) fetching a configuration bit stream for the function; and

(e) programming the FPGA with the configuration bit stream.

11. The medium of claim 10, wherein the issuing instruction (b) comprises the instructions for:

(b1) receiving the instruction by an Auxiliary Processing Unit (APU) interface between the processor and the coprocessor.

12. The medium of claim 11, wherein the determining instruction (c) comprises the instructions for:

(c1) determining that the APU interface issued a faulty commit.

13. The medium of claim 10, wherein the fetching instruction (d) comprises the instructions for:

(d1) initiating an exception subroutine by the processor; and

(d2) fetching the configuration bit stream for the function by an exception subroutine of the processor.

14. The medium of claim 13, wherein the initiating instruction (d1) comprises the instructions for:

(d1i) determining that the coprocessor issued a faulty commit; and

(d1ii) branching to the exception subroutine by the processor in response to the

faulty commit.

15. The medium of claim 13, wherein the fetching instruction (d2) comprises the instructions for:

(d2i) decoding a function identifier by the exception subroutine;

(d2ii) requesting and being granted ownership of the function;

(d2iii) fetching the configuration bit stream for the function from a memory;

(d2iv) identifying an exception type and a coprocessor instruction type for the configuration bit stream; and

(d2v) sending the configuration bit stream to the coprocessor.

16. The medium of claim 10, wherein the programming instruction (e) comprises the instructions for:

(e1) performing a sequence of load and store instructions by an exception subroutine of the processor to program the FPGA with the configuration bit stream.

17. The medium of claim 10, further comprising the instructions for:

(f) receiving a reissuance of the instruction by the coprocessor.

18. A computer readable medium with programming instructions for dynamically programming Field Programmable Gate Arrays (FPGA) in a coprocessor, the coprocessor coupled to a processor, comprising the instructions for:

(a) beginning an execution of an application by the processor;

(b) receiving an instruction from the processor by the coprocessor to perform a function for the application;

(c) issuing a faulty commit when the FPGA in the coprocessor is not programmed with logic for the function;

(d) initiating an exception subroutine by the processor in response to the faulty commit;

(e) fetching a configuration bit stream for the function by the exception subroutine; and

(f) performing a sequence of load and store instructions by the exception subroutine to program the FPGA with the configuration bit stream.

19. A system, comprising:

a processor for executing an application;

a coprocessor coupled to the processor, the coprocessor comprising Field Programmable Gate Arrays (FPGA); and

a memory coupled to the processor and the coprocessor, the memory comprising at least one configuration bit stream for a function,

wherein an instruction is issued to the coprocessor by the processor to perform the function for the application during execution of the application,

wherein the coprocessor determines that the FPGA is not programmed with logic for the function,

wherein the at least one configuration bit stream for the function is fetched,

wherein the FPGA is programmed with the at least one configuration bit stream.